**Ex. No:5 Date: 4-09-2020**

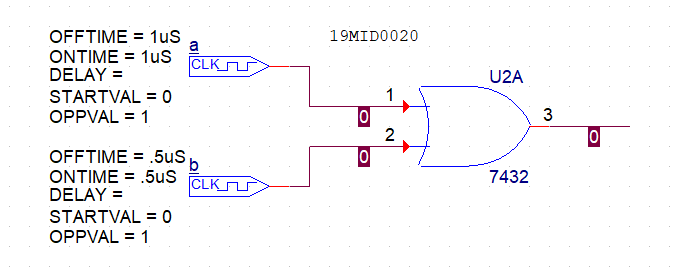
**Implementation and Simulation of Digital Logic Gates & Verifying Boolean Expression Using Truth Table**

**Aim:** To draw the logic circuit diagrams for logic gats and simulate the waves and to verify the given Boolean expression using truth table.

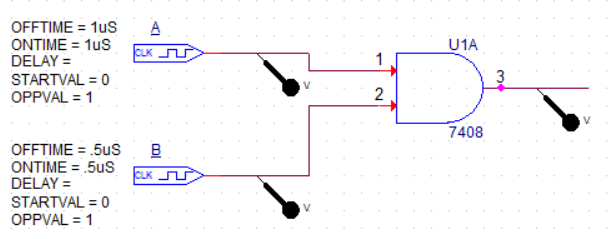
**Apparatus/Tool required:**

ORCAD / PSpice simulator - > **7400 Library – 7432, 7408, 7404, 7400, 7402 & 7486**Source Library – Digclock  
Simulation Settings: Analysis Type - Time Domain  
Run to time: 2us (Logic Gates)  
Run to time: 4us (Boolean Expression)

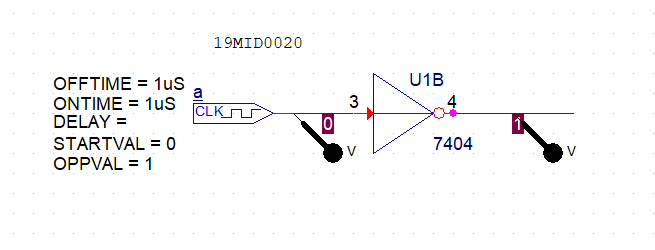
**Circuit Diagram:**

**OR Gate Circuit:**

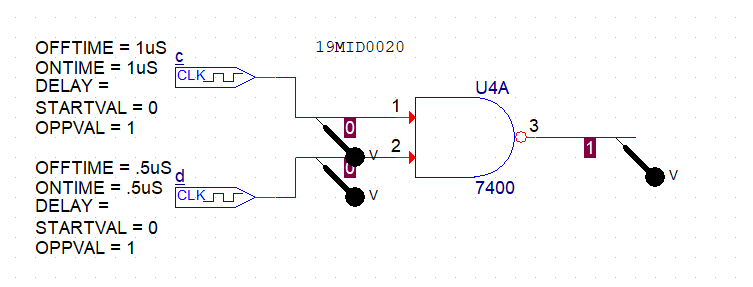
**AND Gate Circuit**



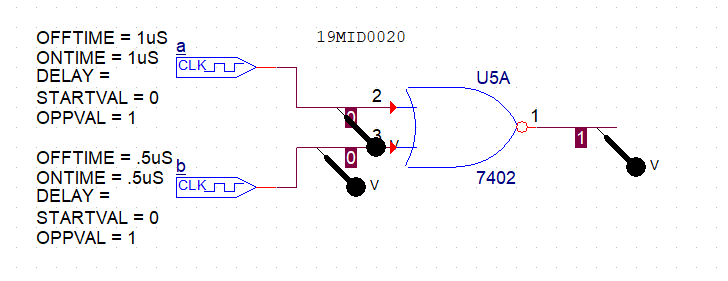
**NOT Gate Circuit :**

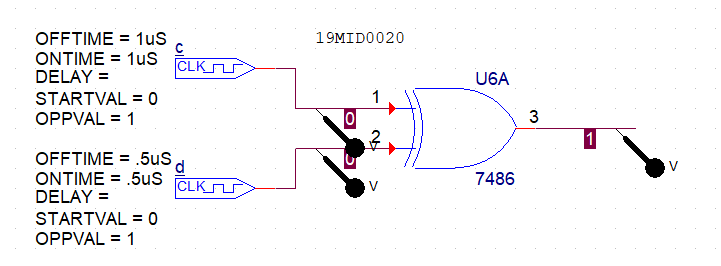


**NAND Gate Circuit:**

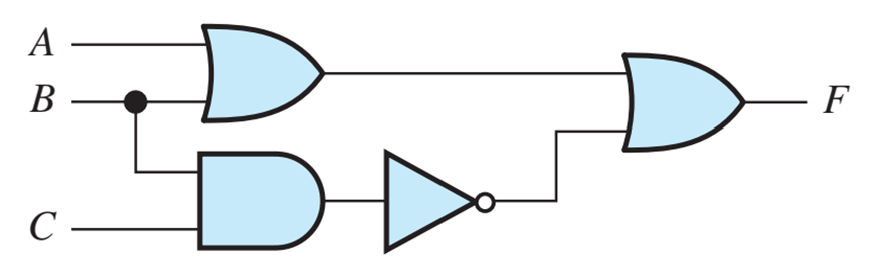


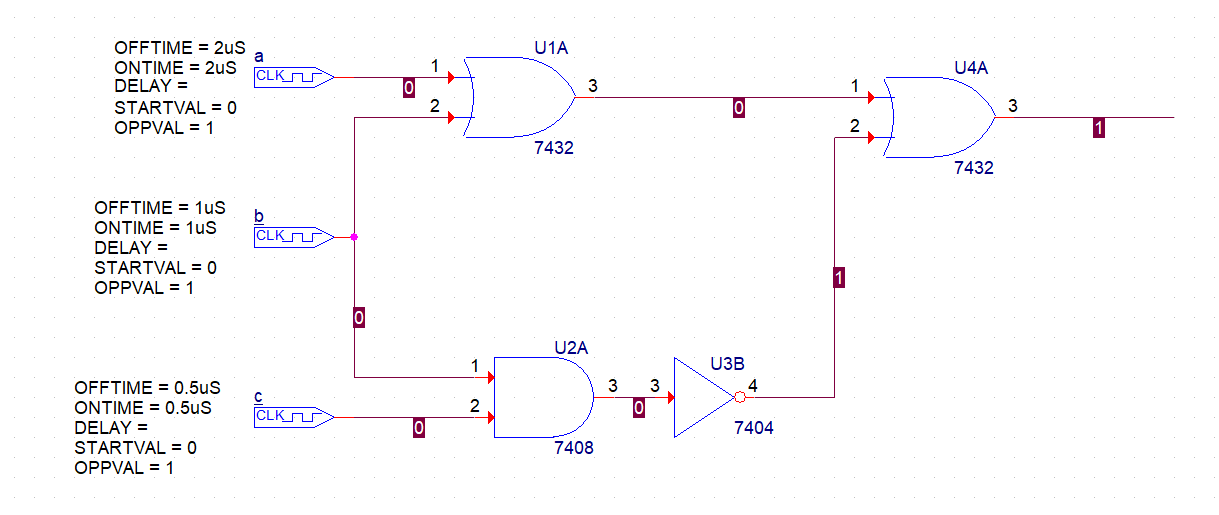
**NOR Gate Circuit:**



**XOR Gate Circuit**

**Write a Boolean expression for the output of the logic circuit. Also, give the truth table for the circuit**





**Theory:**

**OR Gate Circuit: Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| **0** | **0** | **0** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **1** |

**AND Gate Circuit: Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| **0** | **0** | **0** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

**NOT Gate Circuit: Truth Table**

|  |  |
| --- | --- |
| **A** | **Y** |
| **0** | **1** |
| **1** | **0** |

**NAND Gate Circuit: Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| **0** | **0** | **1** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

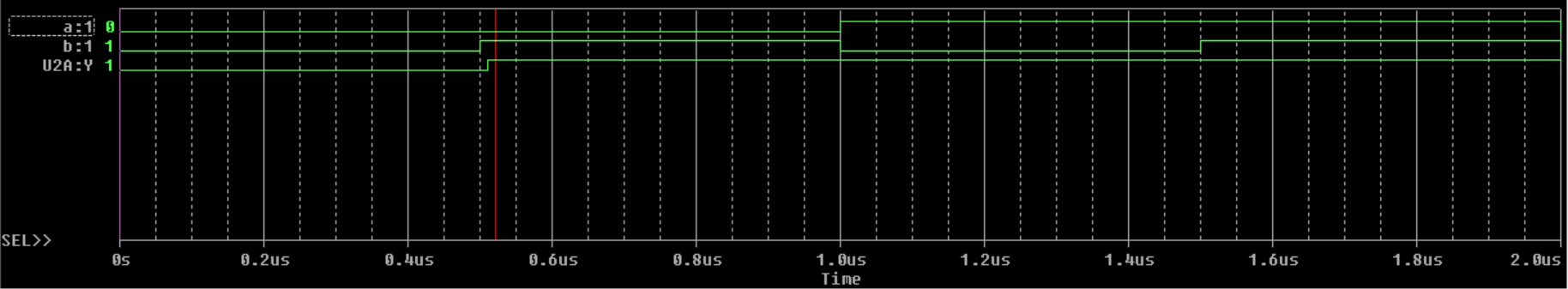
**NOR Gate Circuit: Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| **0** | **0** | **1** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **0** |

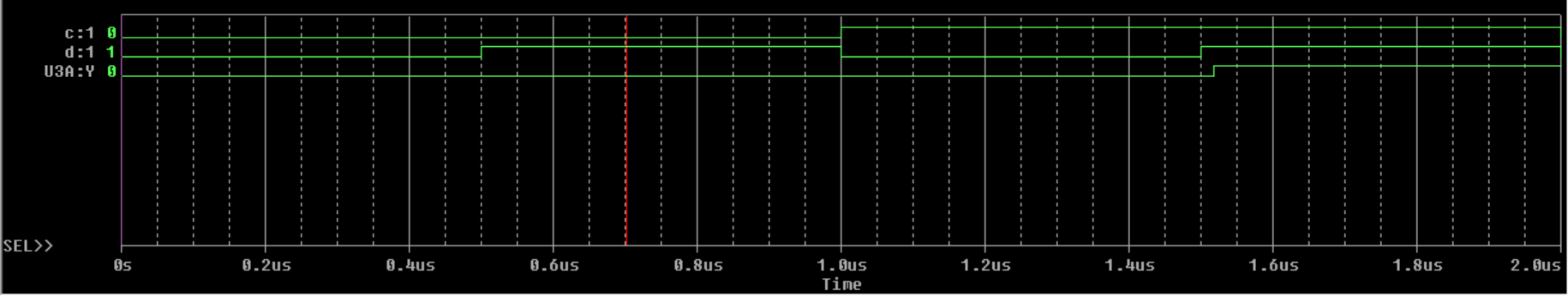
**XOR Gate Circuit: Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| **0** | **0** | **0** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

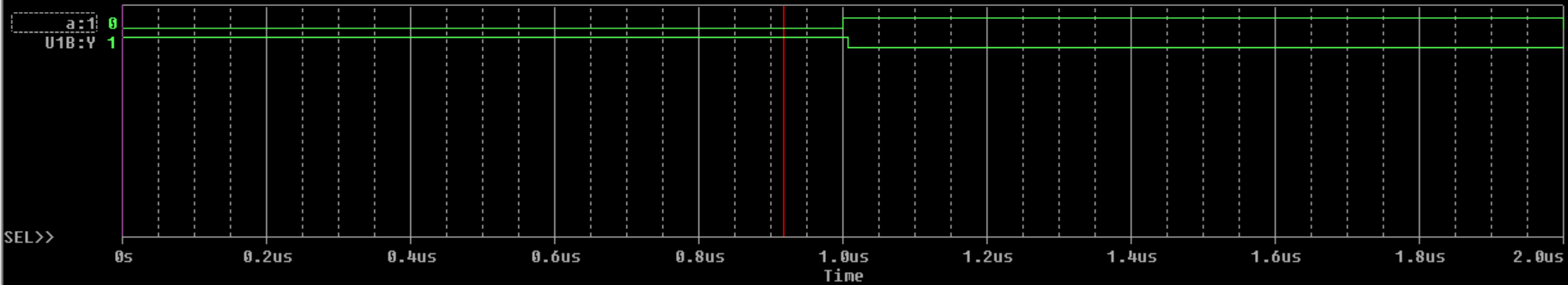
**Practical Circuit and output for OR gate**



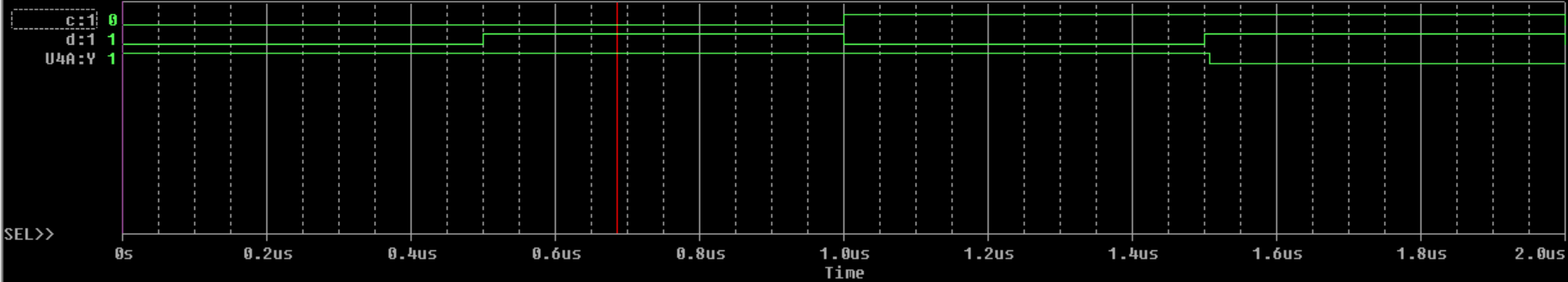
**Practical circuit and output for AND gate**



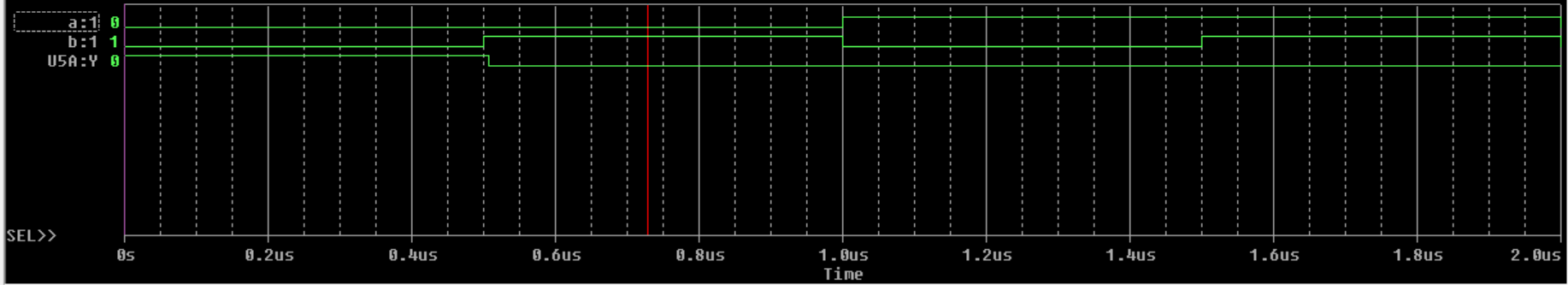
**Practical circuit and output for NOT gate**



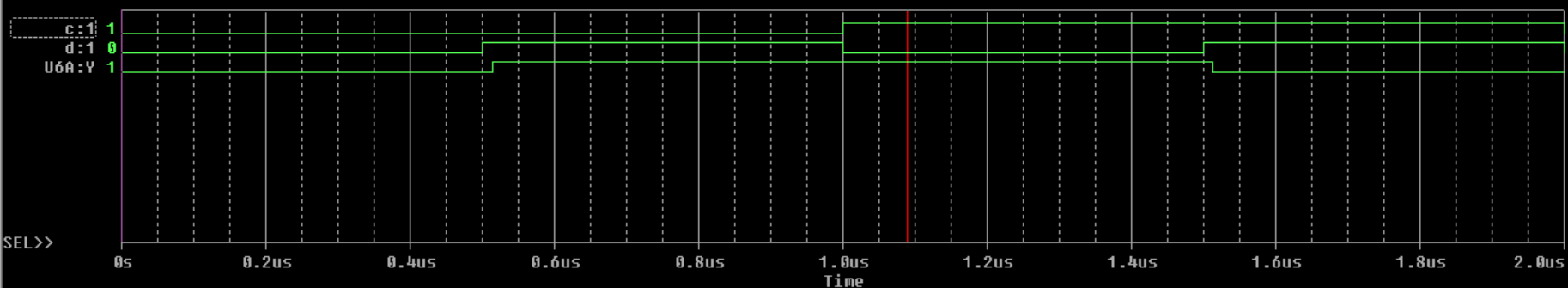
**Practical circuit and output for NAND gate**



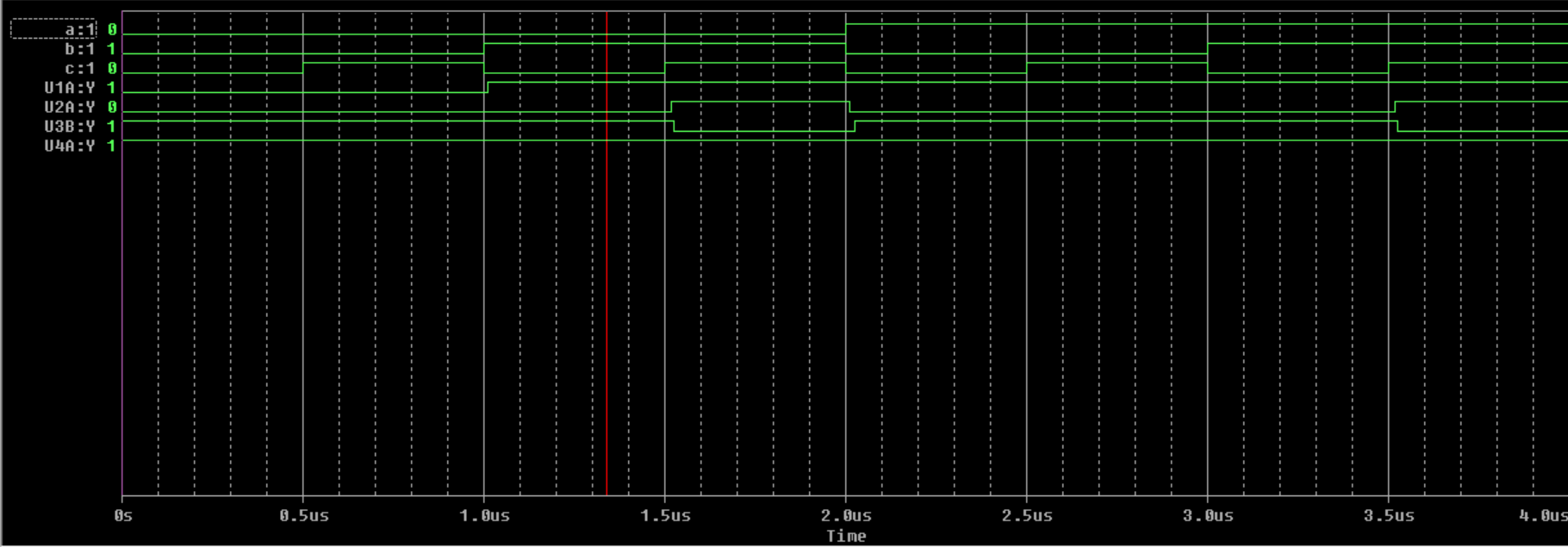
**Practical circuit and output for NOR gate**



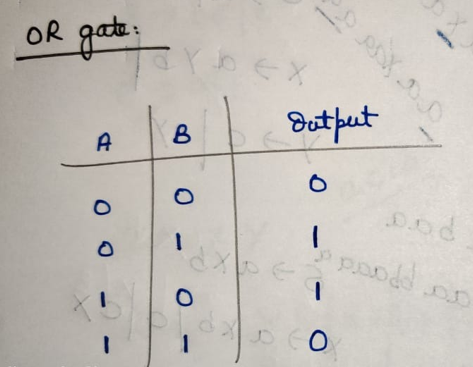
**Practical circuit and output for XOR gate**



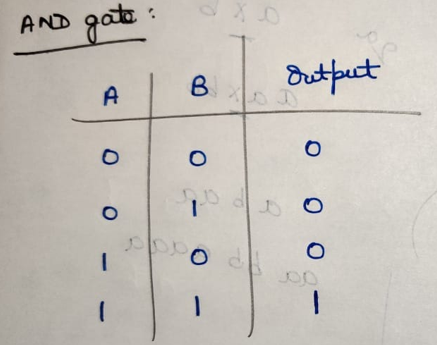
**Practical circuit and output for the Boolean expression**

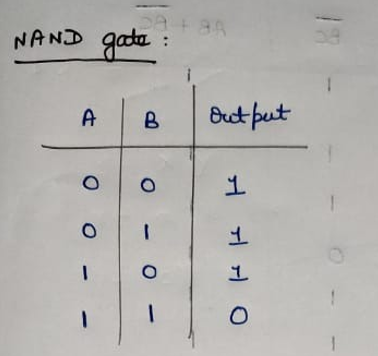


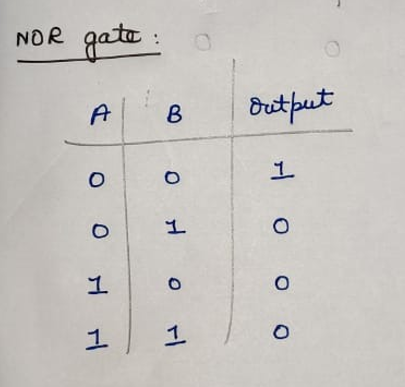
**Manual calculations**

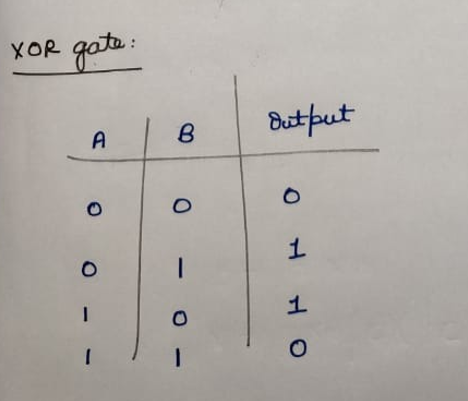


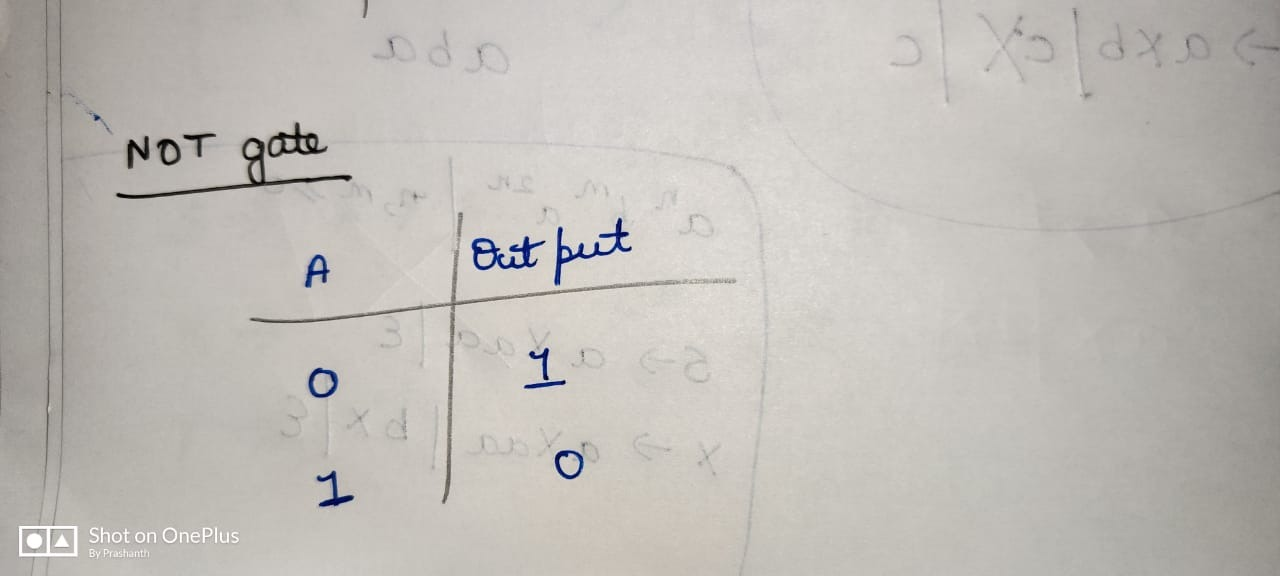






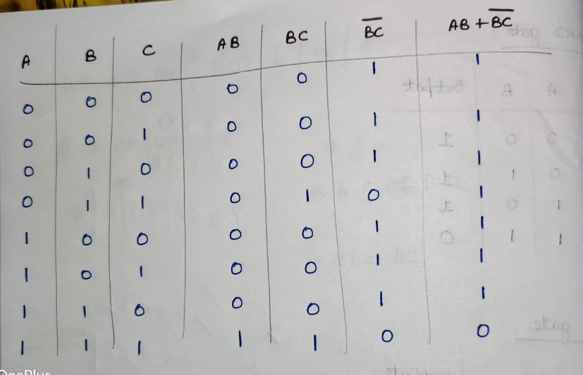






**F = AB + BC**







**Procedure :**

1)Draw the logic circuit for all the logic gates using Orcad pcb designer lite software, with a time difference of 0.5 micro seconds.  
2)Run and get the simulation for all operations ( Keep the run time as 2 micro seconds)

3) Similarly draw the circuit diagram for the given Boolean expression.

4) And get the simulation for the Boolean expression (keep the run as 4 micro-seconds)

5) Draw the truth table with the help of the simulation wave by changing the input values by using the toggle key option and verify it with theoretical values.

6) Libraries need to be added: EVAL 🡪 digclock

**Result**

The theoretical values and the simulated results are same for logic gates and Boolean expressions.

**Inferences :**

The theoretical values and the simulated results are same, hence the logic gates and Boolean expressions are verified.

